REMARKS

Status of the Claims

- Claims 1-7 and 9-29 are pending in the Application.
- Claims 1-7 and 9-29 are rejected by Examiner.
- Claims 1, 13, 22 and 28 are amended by Applicant.

Telephone Interview

Applicant thanks Examiner's Supervisor, Ulka Chauhan, for granting a telephone interview on September 6, 2005. During that interview, the Examiner's supervisor indicated that the current amendment most likely overcomes the current 35 U.S.C. §103(a) rejection. However, another search may be required for further prosecution. Applicant awaits a final decision on whether an additional search is required by the Office.

Claim Rejections Pursuant to 35 U.S.C. §103

Claims 1-7 and 9-28 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent Application Publication No. 2002/0196256 to Hoppe et al. in view of U.S. Patent No. 6,252,612 to Jeddeloh. Applicant respectfully traverses the rejection.

Hoppe et al. teaches a system and method to effect the reduction of aliasing artifacts along discontinuity edges of a rendered polygon mesh by overdrawing the edges as antialiased lines. The processes of Hoppe et al. are targeted to be effective at reducing the temporal artifact known as "crawling jaggies". (Abstract)

Hoppe et al. also teaches a graphics computing device in Figure 2 that includes a central processing unit (CPU), a system memory, a graphics processing unit (GPU) and a frame buffer that forms the video memory. (Figure 2 and para. 0034.)

Hoppe et al. states in paragraph 0040 that:

> *"The GPU 206 includes a rendering module* 240 and an overdrawing module 242, which can be implemented in hardware or a combination of hardware and software. *The rendering module 240 renders the triangles from the mesh 232 and places the rendered images in the frame buffer 208."* (para. 0040)

Applicant submits that the GPU of Hoppe et al. places the rendered images into the frame buffer.

Jeddeloh teaches a multiple memory controller system, comprising at least two memory controllers, wherein one of the at least two memory controllers comprises an accelerated graphics port and at least one configuration register defining a preferred range of addresses that are used for accelerated graphics port transactions. (Abstract).

Specifically, the Examiner cites col. 4 lines 35-40 which state:

"In contrast to the direct memory access (DMA) model where graphics data is copied from the main memory 156 into the local frame buffer 162 by a long sequential block transfer prior to use, *the graphics accelerator 160 of the present invention can also use, or "execute," graphics data directly from the memory in which it resides* (the "execute" model)." (col. 4 lines 35-40).

Applicants submit that the graphics accelerator of Jeddeloh uses graphics data directly from the memory in which it resides.

Applicants have amended independent Claim 1 in accordance with paragraph 0035 of the specification. Amended Claim 1 recites:

> A method for rendering graphics on a display device for a computer system having a central processing unit, system random access memory, and a graphics card, said graphics card comprising a graphical processing unit, video random access memory, and a frame buffer, said method comprising:
>
> rendering a graphic in the system random access memory with the central processing unit; and
>
> *copying said graphic from the system random access memory directly into the frame buffer by the central processing unit, wherein copying directly into the frame buffer bypasses the graphical processing unit.*

Hoppe et al. teaches using a GPU to place rendered images into a frame buffer. Hoppe et al. does not use a CPU to accomplish this function. Jeddeloh employs a graphics processor to use graphics data directly from the memory in which it resides. Jeddeloh does not use a CPU to accomplish this function.

Both Hoppe et al. and Jeddeloh, considered either separately or combined, fail to teach or suggest copying said graphic from the system random access memory directly into the frame buffer by the central processing unit, wherein copying directly into the frame buffer

bypasses the graphical processing unit. In fact, Hoppe et al. and Jeddeloh both teach away from amended Claim 1. Hoppe et al. requires the use of a GPU and Jeddeloh requires the use of a graphics accelerator whereas amended Claim 1 recites that the GPU is bypassed.

Since both Hoppe et al. and Jeddeloh teach away from amended Claim 1 and fail to teach or suggest copying said graphic from the system random access memory directly into the frame buffer by the central processing unit, wherein copying directly into the frame buffer bypasses the graphical processing unit, then neither Hoppe et al. nor Jeddeloh, considered either separately or combined, can render obvious amended independent Claim 1.

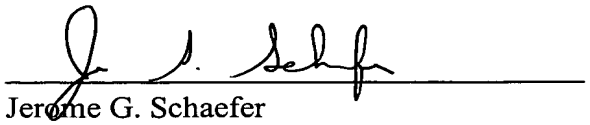
Independent Claims 13, 22 and 28 are similarly amended by Applicant and thus similarly may be distinguished from the cited art. Accordingly, Applicant respectfully requests withdrawal of the §103(a) rejection and submits that amended independent Claims 1, 13, 22 and 28 patentably define over the cited art. Applicant also respectfully requests withdrawal of the §103(a) rejection on the respective dependent claims as they also patentably define over the combination of Hoppe et al. and Jeddeloh.

Conclusion

In view of the above amendments and remarks, Applicant submits that the present application is in a condition for allowance upon entry of the amendments herein. Applicant respectfully and earnestly solicits a Notice of Allowance for all pending claims.

Respectfully submitted,

Date: September 8, 2005



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